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Sub Threshold SRAM Design for Ultra Low Power Applications

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Abstract— Memory unit is the basic building block for any processor.RAM acts as a memory unit in most of the applications .By scaling of technology and varying the voltage values, various parameters such as power consumption, leakage power and delay varies. The purpose of this paper is to implement SRAM cell with different number of transistors in various CMOS technologies such as 180nm and 90nm and to analyze variation in parameters such as power consumption, leakage power and delay operations using CADENCE VIRTUOSO tool.

Index Terms— SRAM, Power Dissipation, Delay.

I. INTRODUCTION

In general, the term RAM refers solely to solid-state memory devices (either DRAM or SRAM), and more specifically the main memory in most computers.

Static Random Access Memory(SRAM) remain to be one of the most paramount and integral memory technologies today mainly because of their robustness and ease at manufacturing. This form of memory is used as cache memory in CPU as it is faster and consumes less power than DRAM which stores a bit of data using a transistor and capacitor pair.

Both SRAM (static RAM) and DRAM (dynamic RAM) are considered volatile, as their state is lost or reset when power is removed from the system. SRAM is more expensive and less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers. SRAM and DRAM holds data but in a different ways. DRAM requires the data to be refreshed periodically in order to retain the data. SRAM does not need to be refreshed as the transistors inside would continue to hold the data as long as the power supply is not cut off. This behavior leads to a few advantages, not the least of which is the much faster speed that can be written and read simultaneously.

SRAM is used in personal computers, work stations, routers and peripheral equipments such as CPU register files, internal CPU caches and external burst mode SRAM caches, hardisk buffers, router buffers, etc. LCD screens and printers also employ static RAM to hold the image displayed.

For many years together, the CMOS devices have been downsized to improve the speed, performance and achieve ultra-low power consumption as they have become prominent in usage for many applications, for instance communications.

Because of the high speed, SRAM based system on chips and cache memories are frequently used. As the number of transistors being used increases, power consumption becomes a major concern. Thus substantial attention has to be paid to design low power and high performance SRAM cells. Many designs are coming out to do so. In this paper various transistor models are proposed such as 4T, 6T and 8T and their performance characteristics are compared.

II. SRAM ARCHITECTURE

An SRAM cell can be in Standby wherein the circuit is idle, Reading when the data has been requested or Writing when updating the contents. Now considering each case, Standby is when word line is not asserted, the access transistors disconnect the cell from the bit lines. The two cross-coupled inverters formed continue to sustain each other as long as they are disconnected.

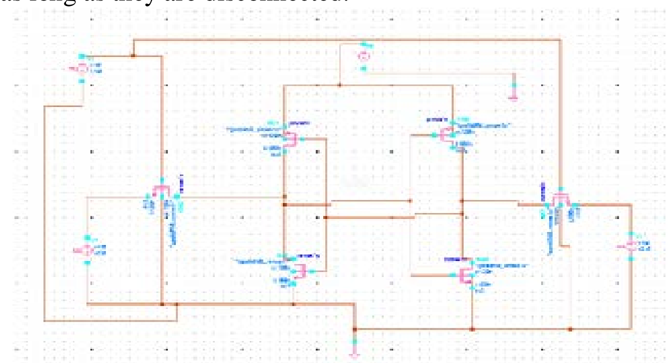

Fig1 : 6T SRAM

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Table 1: Sizing of transistors of 6T SRAM cell

Transistor	Length	Width
PM0,PM1	90nm	120
NM0,NM1	90nm	600
NM2,NM3	90nm	120

Transistor	Length	Width
PM0,PM1	180nm	400
NM0,NM1	180nm	400
NM2,NM3	180nm	400

Write operation is carried out and the value to be written is applied to the bit-lines to start the writing operation. To write a 0, we would apply a 0 to the bit lines, i.e. setting –BL= 1 and BL= 0. This is similar to a causing the flip-flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in [3]. The main reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters [2]. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation depending on the technology being used.

In case of Read operation lets assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and -Q are transferred to the bit lines by leaving BL at its pre-charged value and discharging -BL through one side of transistors to a logical 0. On the BL side, the transistors on the other side pull the bit line toward VDD, a logical 1. If the content of the memory was a 0, the opposite would happen and -BL would be pulled toward 1 and BL toward 0.This justifies that the read operation

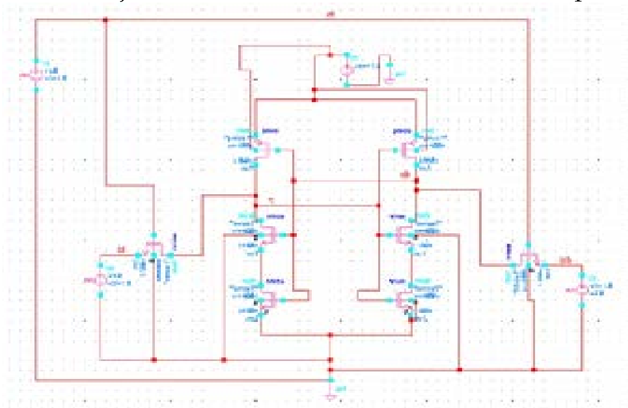

Fig2: 8T SRAM

Table 2: Sizing of transistors of 8T SRAM cell

Transistors	Length	Width
PM0,PM1	90nm	240,240
NM0,NM1,NM3	90nm	600,120,120
NM4,NM5,NM6	90nm	120,120,240

Transistors	Length	Width
PM0,PM1	180nm	400
NM0,NM1,NM3	180nm	400
NM4,NM5,NM6	180nm	400

The operation of 8t SRAM cell is same as that of 6t instead here we use two additional transistors ,one each in pull down path of cross coupled inverters in order to achieve leakage power reduction.

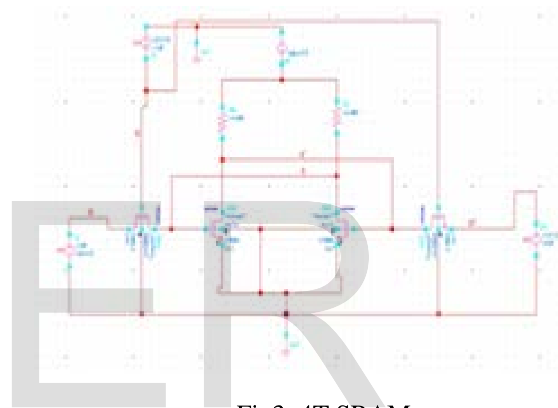

Fig3: 4T SRAM

The 4t SRAM cell comprise of four transistors and two resistors. The resistors R0 and NM2 divide the voltage between VDC and ground. When NM2 is in high impedance state, then the voltage differential falls off almost entirely at NM2, so that the connection between R0 and NM2 is at VDC[5]. In that case, NM3 is enabled and therefore in low impedance state. As a result, the voltage level between R1 and NM3 is close to ground. This in turn disables NM2, which remains in high impedance. If however NM2 is in low impedance, then the roles of NM2 and NM3 are reversed. We have seen that there exist two stable states, one with NM2 in high impedance and one with NM3 in high impedance.

Transistors NM0 and NM1 lead to two complimentary bit lines. If they are enabled, then one of the bit lines will be driven to VDC and the other one to GND. This allows reading of the SRAM cell. If one of them is driven to VDC and the other one to GND, and if then the transistors NM0 and NM1 are enabled and then disabled, the SRAM cell will stay in the state imposed on it by the bit lines. This is the write process of the SRAM cell.

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The 4T design has a certain amount of current leakage on the lines from ground to VDC. For this reason, we can use transistors in lie of the resistors.

Table 3: Sizing of transistors of 4T SRAM cell

Transistor	Length	Width
NM0,NM1	90nm	600,120
NM2,NM3	90nm	120,240

Transistor	Length	Width
NM0,NM1	180nm	400,400
NM2,NM3	180nm	400,400

III. EXPERIMENTAL RESULT

The output response of q and q' are obtained by altering the properties such as pulse width, time period of the inputs i.e., bl, bl' and wl.

6T OPERATION:

Bit lines are connected to the access transistors when we give different pulse widths and we get four cases when wl=0 no operation takes place. When wl is enabled the operations that take place are

Table 4: Operation of 6T SRAM

BL	BLB	Q	Operation
0	0	0	
0	1	0	Write (0)
1	0	1	Write (1)
1	1	Previous Value	Read

Fig4: Transient Response of 6T SRAM

Table 4: Performance characteristics of 6T 90nm

6T (90nm)			
VDD	POWER CONSUMPTION(W)	LEAKAGE POWER(W)	DELAY(s)
0.8	6.114E-6	21.06E-9	500.6E-12
0.7	3.814E-6	16.96E-9	600.2E-12
0.6	2.106E-6	11.28E-9	2.055E-9
0.5	949.8E-9	5.031E-9	3.866E-9
0.4	293.1E-9	2.819E-9	4.317E-9

As the voltage value is increased, power consumption values and leakage power values are decreased whereas delay to produce output is decreased [2].

The power consumed and the leakage power values are more when 6T is implemented using 180nm technology.

8T OPERATION:

The operation of 8T SRAM cell is similar to 6t SRAM cell , the only difference is that here tow extra transistors are used to decrease the leakage power[1]. Same inputs are considered here in order to get the four cases as in table 1 i.e. No operation, Write (0), write (1) and read cases

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Table 5: Performance characteristics of 6T in 180nm

6T (180nm)			
VDD	POWER CONSUMPTION(W)	LEAKAGE POWER(W)	DELAY(s)
1.8	349.8E-6	428.0E-6	1.707E-9
1.5	200.6E-6	212.09E-6	1.123E-9
1.2	92.47E-6	3.765E-6	138.2E-12
1	44.12E-6	9.91E-9	53.23E-12
0.8	14.15E-6	4.11E-9	15.61E-12

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Fig5 : Transient Response of 8T SRAM

Table 6: Performance characteristics of 8T in 90nm

8T(90nm)			
VDD	POWER CONSUMPTION(W)	LEAKAGE POWER(W)	DELAY(s)
0.8	8.39E-6	4.931E-6	657.4E-12
0.7	5.27E-6	2.59E-6	934.2E-12
0.6	2.87E-6	860.3E-9	2.583E-9
0.5	1.25E-6	704.9E-9	4.34E-9
0.4	361.2E-9	4.65E-9	5.261E-9

With the scaling of voltage values power consumption and leakage power decreases whereas 8T has more speed at 0.8v as compared to lower voltage values.

Table 7: Performance characteristics of 8T in 180nm

8T (180nm)			
VDD	POWER CONSUMPTION(W)	LEAKAGE POWER(W)	DELAY(s)
1.8	143.0E-6	11.33E-6	370.0E-12
1.5	82.74E-6	25.6E-9	643.2E-12
1.2	39.4E-6	7.57E—9	2.033E-9
1	19.79E-6	2.14E-9	1.771E-9
0.8	7.30E-6	1.377E-9	1.369E-9

From the above tabulated values, it can be inferred that the power consumed by the 8T SRAM cell is lower compared to that of 6T SRAM cell.

4T OPERATION:

In the case 4t SRAM cell the two PMOS transistors are replaced by two resistors and because of these two resistors the power consumption and leakage power is slightly higher than the other proposed models

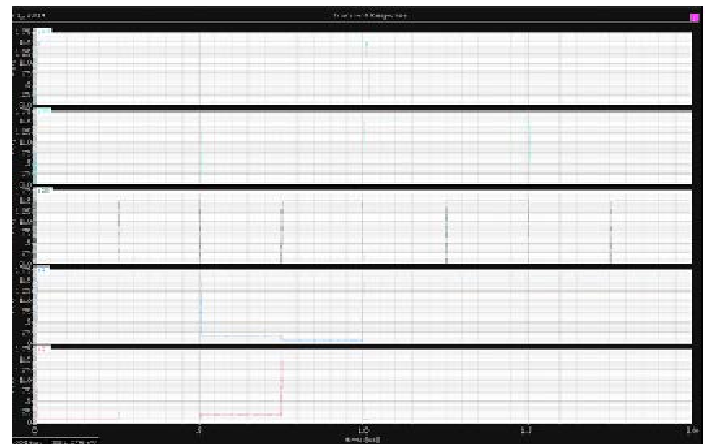

Fig6: Transient Response of 4T SRAM

From the table 8, we can conclude that the power consumption and leakage power of 4T are high compared to 6T and 8T because of the load resistors. The advantage of 4T SRAM is that it occupies lesser space than other SRAM cells.

Table 8: Performance characteristics of 4T in 90nm

4T(90nm)			
VDD	POWER CONSUMPTION(W)	LEAKAGE POWER(W)	DELAY(s)
0.8	36.34E-6	4.787E-6	245.03E-9
0.7	24.03E-6	3.088E-6	245.08E-9
0.6	12.67E-6	2.448E-6	245.1E-9
0.5	4.771E-6	1.525E-6	245.215E-9
0.4	1.339E-6	534.7E-9	245.324E-9

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Table 9: Performance characteristics of 4T in 180nm

4T(180nm)			
VDD	POWER CONSUMPTION	LEAKAGE POWER	DELAY
1.8	388.8E-6	353.5E-6	395.1E-12
1.5	261.5E-6	217.8E-6	1.486E-9
1.2	158.3E-6	132.1E-6	1.315E-9
1	102.6E-6	88.86E-6	1.834E-9
0.8	55.3E-6	50.24E-6	2.118E-9

We can observe that there is a huge difference in power values whereas 4T SRAM cell in 180nm is faster than 4T SRAM cell in 90 nm.

IV.CONCLUSIONS AND FUTURE SCOPE

In this paper, a study on the state of SRAM cell and technologies and different performance metrics has been done. It has been analyzed that SRAM cell in 90nm technology is better than 180nm in terms of all the parameters .An efficient SRAM cell in both the aspects power consumptions and speed in terms of delay is implemented and explained.

This can be further implemented in other technology by scaling the CMOS technologies and analyzing the various parameters in order to determine the performance of SRAM cells and the same bit cells can be used to design arrays of SRAM.

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